# Lab 2: Design an ALU

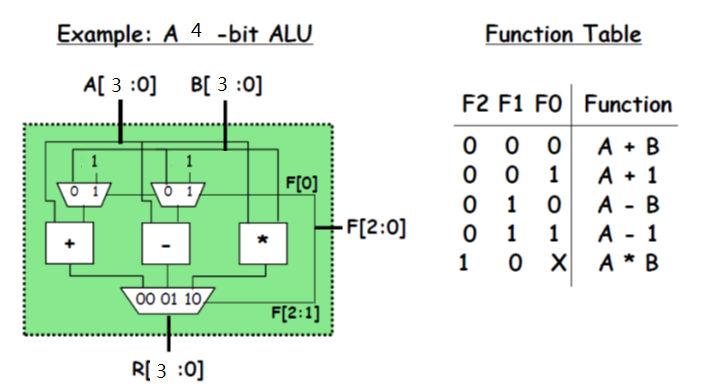
(2+2 hours)

## Goal

To learn how to use the behavior model Verilog HDL description to design and implement an ALU.

## Procedure

Design an ALU with the following functions. Refer to slides of Lecture 3.



1. Design the modules of 4-bit 2-1 Mux, 4-bit 3-1 Mux, 4-bit Adder, 4-bit Subtracter, and 4-bit Multiplier. You do not need to consider the situation of overflow.
2. Design the top module for the ALU with hierarchy structure of the modules defined in step 1).
3. Implement the design in FPGA, with the data input A[3:0], B[3:0], and the control input F[2:0] connected to the switches on Basys3 board, and the output R[3:0] to the LEDs on board.
4. (optional) Try to solve the overflow problem in this design with your own method.
5. (optional) Try to extend the Function table with new functions.